



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/077,189	02/15/2002	Tong Liu	ACT-322	2718

7590 10/03/2003
Michael A. Blake
Sierra Patent Group, Ltd.
P.O. Box 6149
Stateline, NV 89449

EXAMINER

THOMPSON, ANNETTE M

ART UNIT PAPER NUMBER

2825

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/077,189

Applicant(s)

LIU ET AL.

Examiner

A. M. Thompson

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 February 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 8-16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 February 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6.
- 4) ☒ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This application 10/077,189 has been examined. Claims 1-16 are pending.

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-7, drawn to the structure and layout of a FPGA, classified in class 326, subclass 41.
 - II. Claims 8, 9, 15, 16, drawn to a method of routing the internal components of a FPGA tile, classified in class 716, subclass 12.
 - III. Claims 10-14, drawn to a method of designing an FPGA freeway interconnect structure, classified in class 716, subclass 1.

The inventions are distinct, each from the other because of the following reasons:

Inventions I, II, and III are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case Invention I recites the overall structure of a FPGA; Invention II recites the details of routing the internal components of a FPGA tile; and Invention III recites the design of a FPGA structure. Although all three inventions relate in some way to freeway architecture, the inventions disclose different functions and independent operations relating to freeway architecture and the inventions are not necessarily required or capable of being used together.

2. During a telephone conversation with Mr. William Wilbar, 43,265 on 16 September 2003, a provisional election was made without traverse to prosecute the

Art Unit: 2825

invention of Group I, claims 1-7. Affirmation of this election must be made by Applicants in replying to this Office Action. Claims 8-16 are withdrawn from further consideration by the Examiner, 37 CFR 1.142(b), as being drawn to non-elected inventions.

3. Applicants are reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

4. The drawings are objected to based on the following reasoning: In addition to the Draftperson's PTO-948, Figures 6 and 13 include unlabeled I/O. In Figures 16A and 16B, the tristate buffer pins are unconnected. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The

disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

6. The abstract of the disclosure is objected to because it contains claim language and it is greater than 150 words. Correction is required. See MPEP § 608.01(b).

7. The disclosure is objected to because of the following informalities: At page 1, the first 5 lines contain information which should not be part of Applicants' specification or disclosure. The declaration submission and assignment papers already account for this information. Additionally, at page 1, insert current status of referenced application, e.g. - -now U.S. Patent. . .- -. Further, with reference to the additional application numbers referenced throughout the specification, Applicant is required to insert the current status of those applications at all listed occurrences.

Appropriate correction is required.

Claim Objections

8. Claims 1-7 are objected to for the following reasons: Pursuant to claim 1, the preamble recites a freeway routing system, however, the remainder of the claim limitations is directed to a FPGA structure, not a system. Claims 2-7 are dependent from claim 1 and are likewise rejected. Pursuant to claim 2, at line 5, change "any" to - -an- -. Pursuant to claims 4 and 5, "first FPGA tile" lacks antecedent basis. Replacing "said" with - -a- - would overcome this objection. Pursuant to claim 6, "IO" should be changed to - -IG- - to provide structural /functional relationship with the remainder of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the **first** paragraph of 35 U.S.C. 112:

Art Unit: 2825

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Pursuant to claim 1, it recites the limitation of the IGs having a first, second and third set of input and output ports is not specifically disclosed in the specification. Although this limitation is recited verbatim in the specification, no further mention of configuring or using the IGs in his manner is disclosed in the specification. For examination purposes, the recitation of this limitation (only) is not treated. Claims dependent from claim 1 are likewise rejected to the extend that this limitation is included therein.

11. The following is a quotation of the **second** paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 2, 3, 6, and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

13. Pursuant to claim 2, the phrase "FPGA tile configured" is confusing because there is no prior recitation of configuring an FPGA tile; furthermore, there is no prior recitation of a "first FPGA". Pursuant to claim 6, no structural/functional relationship exists between the "IO" and the rest of claim 1; in fact, claim 1 does not even mention IO. Pursuant to claim 7, no structural/functional relationship exists between the "RAM"

Art Unit: 2825

and the rest of claim 1; claim 1 does not even mention the FPGA comprising any sort of memory.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Rejection of claims 1-7

15. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kaptanoglu, U.S. Patent 6,285,212. Kaptanoglu discloses a FPGA architecture.

16. Pursuant to claim 1, Kaptanoglu discloses a FPGA comprising a plurality of FPGA tiles comprising a plurality of functional groups arranged in rows and columns (Fig. 2; col. 2, ll. 28-37; col. 3, ll. 1-12); a plurality of interface groups surrounding the plurality of FGs (col. 2, ll. 30-33; Fig. 1, #14) such that one IG is positioned at each end of each row and column; a freeway set of routing conductors configured to transfer signals (col. 2, ll. 28-37); said freeway set of routing conductors comprising a plurality of vertical conductors that form intersections with a plurality of horizontal conductors and programmable interconnect elements (col. 6, line 60 to col. 7, line 16) located at said intersections in a diagonal orientation on said FPGA tile (col. 8, line 66 to col. 9, line 4; col. 10, ll. 6-21).

17. Pursuant to claim 2, where there are other FPGA tiles similar to the first FPGA tile (Fig. 1, illustrates multiple FPGA tiles).

18. Pursuant to claim 3, wherein the FPGA further comprises programmable interconnect elements (col. 6, ll. 5-19, the F-tab; col. 7, ll. 4-16, the E-turn) located at the connections between adjacent FPGA tiles.

19. Pursuant to claim 4, wherein the diagonally oriented programmable interconnects are arranged from the upper left corner of a FPGA tile to the lower right corner of the FPGA tile (Fig. 6, #60; col. 10, ll. 51-67; col. 11, ll. 1-22).

20. Pursuant to claim 5, wherein the diagonally oriented programmable interconnects are arranged from the upper right corner of a FPGA tile to the lower left corner of the FPGA tile (Fig. 6, #6; col. 10, line 35 to col. 11, line 22).

21. Pursuant to claim 6, wherein the freeway set of routing conductors are configured to transfer signals from output ports of one IG (col. 4, ll. 31-43; col. 11, ll. 1-22).

22. Pursuant to claim 7, wherein the freeway set of routing conductors are configured to transfer signals from output ports of one RAM (col. 11, ll. 7-22).

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please reference the PTO-892 for a complete listing. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If

Art Unit: 2825

attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703) 306-3329.

24. Responses to this action should be mailed to:

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).



A. M. THOMPSON
Master's Level Patent Examiner